



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Tohru KOYAMA, et al.

Confirmation Number: 7582

Application No.: 10/830,090

Group Art Unit: 2829

Filed: April 23, 2004

Examiner: Arleen M. Vazquez

For: FAILURE ANALYZER

VERIFIED ENGLISH TRANSLATION

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Submitted herewith is the Verified English Translation of: Japanese Patent Application Number JP2003-121282, which was filed in Japanese Language on April 25, 2003.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael A. Messina Registration No. 33,424

600 13th Street, N.W. Washington, DC 20005-3096 Phone: 202.756.8000 MAM:llg

Facsimile: 202.756.8087

Date: November 21, 2007

Please recognize our Customer No. 20277 as our correspondence address.

Attorney Docket:

NOV 2 1 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tohru KOYAMA et al.

)

Filing Date:
April 23, 2004

For: FAILURE ANALYZER)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks Washington D.C. 20231

Patent Application No.

10/830,090

Sir:

Yukiko Tachiwana residing at c/o Yoshida, Yoshidae and Arita Patent Office of Sumitomo-Seimei OBP Plaza Building, 4-70, Shiromi 1-chome, Chuo-ku, Osaka, Japan declares:

- 1) that I know well both the Japanese and English languages;
- 2) that I translated the priority documents of the Japanese Patent Application No. 2003-121282 from Japanese to English;
- 3) that the attached English translation is a true and correct translation of the priority documents of the Japanese Patent Application No. 2003-121282 to the best of my knowledge and belief; and
- 4) that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: Nov. 5, 2007 Signature: Tullo Jackmana

Yukiko Tachiwana



JAPAN PATENT OFFICE

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: April 25, 2003

Patent Application Number: JP2003-121282

Applicant(s): Renesas Technology Corp.

Commissioner,

Japan Patent Office



[Document Name] Patent Application

[Docket Number] 545553JP01

[Filing Date] April 25, 2003

[Directed to] To the Director General of the JPO

[International patent classification] HO1L 21/66

[inventor]

[Domicile] c/o Renesas Technology Corp.
4-1, Marunouchi 2-chome, Chiyoda-ku, TOKYO
[Name] Tohru KOYAMA

[inventor]

[Domicile] c/o Renesas Technology Corp.
4-1, Marunouchi 2-chome, Chiyoda-ku, TOKYO
[Name] Junko KOMOR!

[Applicant of Patent Application]
 [Identification Number] 503121103
 [Name] Renesas Technology Corp.

[Attorney]

[Identification number] 100089233
[Patent Attorney]
[name] Shigeaki YOSHIDA

[Assigned Attorney]

[Identification number] 100088672
[Patent Attorney]
[name] Hidetoshi YOSHITAKE



[Assigned Attorney]

[Identification number] 100088845

[Patent Attorney]

[name] Takahiro ARITA

[Government Fee]

[Ledger Number] 012852

[Fee] 21000 yen

[List of Attached Items]

[Item]

Specification

[Item]

Drawing

[Item]

Abstract of the Disclosure

[Proof of Filing] necessary



[Document Name] Specification

[Title of the Invention] Failure Analyzer

[Claims]

5

10

15

25

[Claim 1] A failure analyzer comprising:

an analysis plate including a first main surface mounting a sample thereon and a second main surface opposite to said first main surface; and

1

a failure detector including an optical system and detecting a failure caused in said sample using said optical system, wherein

a recess is provided in said second main surface of said analysis plate,

a protrusion which does not protrude from said second main surface and functions as a solid immersion lens is provided on a bottom surface of said recess, and

said failure detector irradiates said sample with light through said protrusion from said second main surface side of said analysis plate, or detects light emitted from said sample through said protrusion.

[Claim 2] The failure analyzer according to claim 1, wherein said analysis plate is used as a stage that mounts said sample thereon.

[Claim 3] The failure analyzer according to either of claims 1 and 2, wherein said analysis plate is made of silicon.

[Claim 4] The failure analyzer according to claim 2, wherein said analysis plate is made of quartz glass.

[Claim 5] The failure analyzer according to any one of claims 1 to 4, wherein said second main surface of said analysis plate has a plurality of said recesses formed therein, and

said protrusion is provided on a bottom surface of each of said recesses.

[Claim 6] The failure analyzer according to claim 5, wherein

said sample is a semiconductor wafer having a plurality of semiconductor chips formed therein, and

said recesses and said protrusions are provided in correspondence with said semiconductor chips and provided at positions corresponding to the location of said semiconductor chips.

5

15

25

[Claim 7] The failure analyzer according to claim 5, wherein each of said protrusions is spherical, and said protrusions have locally spherical surfaces with different radiuses.

[Claim 8] The failure analyzer according to any one of claims 1 to 7, further comprising:

a jig for supporting said sample independently of said analysis plate; and
a first driver for moving said analysis plate in parallel with said first main
surface.

[Claim 9] The failure analyzer according to claim 8, further comprising a second driver for moving said optical system of said failure detector in parallel with said first main surface of said analysis plate, wherein

said first driver notifies said second driver of movement information of said analysis plate, and

said second driver moves said optical system based on said movement 20 information.

[Claim 10] The failure analyzer according to any one of claims 1 to 7, further comprising:

a probe needle in contact with said sample on said analysis plate; and
a driver for moving said probe needle and said sample in parallel with said first
main surface of said analysis plate independently of said analysis plate while maintaining

positional relationship between said probe needle and said sample.

[Claim 11] A failure analyzer comprising:

a solid immersion lens;

5

10

15

20

25

a stage including a first main surface and a second main surface opposite to said first main surface and having said solid immersion lens embedded therein; and

a failure detector including an optical system and detecting a failure caused in a sample using said optical system, wherein

a portion of a surface of said solid immersion lens is flat as well as said first main surface of said stage, and is exposed from said first main surface,

said sample is mounted on said first main surface of said stage and on a portion of said surface of said solid immersion lens, and

said failure detector irradiates said sample with light through said stage and said solid immersion lens from the side of said second main surface of said stage, or detects light emitted from said sample through said solid immersion lens and said stage.

[Claim 12] The failure analyzer according to claim 11, wherein said stage is made of quartz glass.

[Claim 13] The failure analyzer according to either of claims 11 and 12, wherein

a protrusion which functions as a convex lens is provided in line with said solid immersion lens in a direction of thickness of said stage in said second main surface of said stage, and]

said failure detector irradiates said sample with light further through said protrusion, or detects light emitted from said sample further through said protrusion.

[Claim 14] The failure analyzer according to any one of claims 11 to 13, wherein said stage has a plurality of said solid immersion lenses embedded therein.

[Claim 15] The failure analyzer according to claim 14, wherein

said sample is a semiconductor wafer having a plurality of semiconductor chips formed therein, and

said solid immersion lenses are provided in correspondence with said semiconductor chips and provided at positions corresponding to the location of said semiconductor chips.

5

15

20

[Claim 16] The failure analyzer according to claim 14, wherein each of said solid immersion lenses is spherical, and

said solid immersion lenses include locally spherical surfaces with different radiuses.

[Claim 17] The failure analyzer according to any one of claims 11 to 16, further comprising:

a jig for supporting said sample independently of said stage and said solid immersion lens; and

a first driver for moving said stage in parallel with said first main surface.

[Claim 18] The failure analyzer according to claim 17, further comprising a second driver for moving said optical system of said failure detector in parallel with said first main surface of said stage, wherein

said first driver notifies said second driver of movement information of said stage, and

said second driver moves said optical system based on said movement information.

[Claim 19] The failure analyzer according to any one of claims 11 to 16, further comprising:

a probe needle in contact with said sample on said stage and said solid

immersion lens; and

a driver for moving said probe needle and said sample in parallel with said first main surface of said stage independently of said stage while maintaining positional relationship between said probe needle and said sample.

5 [Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The invention relates to a failure analyzer utilizing a solid immersion lens.

[0002]

10 [Prior Art]

15

20

25

Ever-increasing use of a multilayer structure for interconnection of a semiconductor device such as an LSI causes difficulties in evaluating or analyzing the semiconductor device from a direction of a top surface of a semiconductor substrate, so that evaluation or analysis of the semiconductor device must be carried out from a direction of a back surface of the semiconductor substrate. Typical techniques for analyzing a failure from a direction of a back surface include: light emission analysis (referred to also as "emission analysis") in which a failures is analyzed by detecting a feeble light emitted from a spot of current leakage; an OBIC (optical beam induced current) analysis or OBRCH (Optical Beam Induced Resistance CHange) analysis in which a failure site is specified by converting a current or change in power supply current which is induced by irradiation of a laser beam into an image; and laser voltage probing (LVP) analysis in which an intensity or phase change of a reflected light provided by irradiation of a laser beam is monitored to observe a waveform of a potential at an arbitrary point. In the above-cited techniques for analyzing a failure from a direction of a back surface of a semiconductor substrate (which will hereinafter be referred to as "back

surface analysis"), an infrared light which can be transmitted through silicon is generally employed because there is a need of accessing a semiconductor device formed on a top surface of a semiconductor substrate with a thickness of several hundred microns via the semiconductor substrate. However, because of the wavelength of the infrared light employed which is equal to 1μ m or larger, an effective spatial resolution is equal to 0.7μ m or higher. As such, there is no choice but to sacrifice improvement in an image resolution to carry out back surface analysis.

[0003]

In view of this, the technique of utilizing a solid immersion lens (which will be hereinafter also referred to as an "SIL") made of silicon is proposed in non-patent document 1 as one method for improving a spatial resolution. This technique is to increase a refractive index of a medium of light, to obtain a resolution which overcomes a diffraction limit defined by a wavelength of the light.

[0004]

According to the technique of non-patent document 1, a substantially hemispherical SIL is provided in close contact with a back surface of a semiconductor substrate, and light transmitted through silicon is caused to be incident upon the semiconductor substrate via the SIL. As a result, a converging angle can be significantly increased as compared to a case where no SIL is provided. The resolution d is represented by an equation, " $d = \lambda / (2 \cdot n \cdot \sin \theta)$ where " $n \cdot \sin \theta$ " represents a numerical aperture NA. Ideally, the numerical aperture NA can be increased to a square of the refractive index (n) by virtue of provision of the SIL. Additionally, " θ " and " λ " in the above equation represent a half angle of the converging angle and the wavelength of the light, respectively.

[0005]

5

10

15

20

Nevertheless, the technique of non-patent document 1 has a disadvantage that a resolution is occasionally reduced considerably due to possible creation of a clearance between the semiconductor substrate and the SIL. Thus, patent document 1 proposes the technique of integrally forming an SIL and a semiconductor substrate by performing some processes on the surface of a semiconductor substrate to form a substantially hemispherical protrusion on the surface of the semiconductor substrate, and then utilizing the formed protrusion as an SIL.

[0006]

5

10

15

The technique of patent document 1, in which the protrusion functioning as an SIL and the semiconductor substrate are formed integrally with each other, prevents creation of a clearance between the SIL and the semiconductor substrate, thereby allowing for improvement in resolution as compared to the technique of non-patent document 1.

[0007]

It is additionally noted that the techniques of utilizing an SIL for back surface analysis of a semiconductor device are also described in non-patent documents 2 and 3.

[8000]

[Patent Document 1]

Japanese Patent Application Laid-Open No. 2002-189000

[Non-patent Document 1]

S.B. Ippolito et al., "High spatial resolution subsurface microscopy", Applied Physics Letters, Vol. 78, No. 26, June 2001, pp. 4071-4073

[Non-patent Document 2]

Terada, "Effectiveness of solid immersion lens", written materials for a lecture of the fourteenth semiconductor workshop sponsored by Hamamatsu Photonics K.K.

25 [Non-patent Document 3]

Yoshida et al., "High Resolution Laser Voltage Probing (LVP)", Proc of LSI testing symposium, 2002, pp. 143-148.

[0009]

5

10

15

20

25

[Problems to be Solved by the Invention]

In general, in carrying out back surface analysis of a semiconductor wafer or a semiconductor chip which is cut out from a semiconductor wafer and not yet packaged, a sample is mounted on a stage transmitting a light with a back surface of the sample being situated downward relative to a top surface of the sample. Then, a probe is brought into contact with an electrode pad provided in the top surface of the sample to place the sample in a conducting state, and subsequently, light is detected from, or irradiated onto, the back surface of the sample via the stage.

[0010]

However, the technique described in non-patent document 1 has difficulties in stably mounting the sample on the stage because of inclusion of the substantially hemispherical SIL on the back surface of the semiconductor substrate which protrudes from the back surface of the semiconductor substrate.

[0011]

On the other hand, in the technique of patent document 1, the SIL is formed by digging in the semiconductor substrate and making the back surface thereof locally spherical, so that the SIL does not protrude from the back surface of the semiconductor substrate unlike in non-patent document 1. Accordingly, it is possible to stably mount the sample on the stage. Nevertheless, in patent document 1, the protrusion functioning as an SIL, which is formed by performing some processes on the semiconductor substrate itself, cannot be moved. Thus, it is impossible to move the range of analysis.

[0012]

Thus, the invention is made in view of the aforementioned problems, and its object is to provide a failure analysis technique that is capable of stably mounting a sample on a stage and changing the range of analysis.

[0013]

5

10

20

25

[Means for Solving the Problems]

A first failure analyzer of the invention includes an analysis plate including a first main surface mounting a sample thereon and a second main surface opposite to the first main surface, and a failure detector including an optical system and detecting a failure caused in the sample using the optical system. A recess is provided in the second main surface of the analysis plate. A protrusion which does not protrude from the second main surface and functions as a solid immersion lens is provided on a bottom surface of the recess. The failure detector irradiates the sample with light through the protrusion from a direction of the second main surface of the analysis plate, or detects light emitted from the sample through the protrusion.

15 [0014]

A second failure analyzer of the invention includes a solid immersion lens, a stage including a first main surface and a second main surface opposite to the first main surface and having the solid immersion lens embedded therein, and a failure detector including an optical system and detecting a failure caused in a sample using the optical system. A portion of a surface of the solid immersion lens is flat as well as the first main surface of the stage to be exposed from the first main surface. The sample is mounted on the first main surface of the stage and on the portion of the surface of the solid immersion lens. The failure detector irradiates the sample with light through the stage and the solid immersion lens from a direction of the second main surface of the stage, or detects light emitted from the sample through the solid immersion lens and the stage.

[0015]

5

10

15

20

25

[Embodiments of the Invention]

First Embodiment.

Fig. 1 illustrates the structure of a failure analyzer 100 of a first embodiment of the invention. Fig. 2 is a partially enlarged view of the structure illustrated in Fig. 1. As illustrated in Figs. 1 and 2, the failure analyzer 100 of the first embodiment is a failure analyzer that is capable of carrying out emission analysis on a sample 1, and it includes an analysis plate 2 including an SIL, an SIL driver 10, a failure detector 20, a microscope driver 23, a sample support jig 30, a prober 40 and a tester 50. Figs. 1 and 2 show the sample 1, the analysis plate 2, the sample support jig 30, a stage 11, a chuck 12, and a probe card 41 in section. The stage 11, the chuck 12, and the probe card 41 is described later.

[0016]

Fig. 3 is a plan view of the structure of the sample 1 that is subjected to analysis in the failure analyzer 100. As illustrated in Figs. 1 to 3, the sample 1 is a semiconductor wafer in which a plurality of semiconductor chips 1c are provided. The sample 1 includes a semiconductor substrate 1a and a device forming layer 1b provided on one main surface 1aa of the semiconductor substrate 1a. The device forming layer 1b includes a semiconductor element such as a MOS transistor, an interlayer insulating layer, a contact plug, an interconnect line, and the like which are not illustrated. The semiconductor substrate 1a is a silicon substrate, for example. It is noted that though the semiconductor wafer in which the plurality of semiconductor chips 1c are provided is employed as the sample 1 in an example described herein, each of the semiconductor chips 1c which is cut out from the semiconductor wafer can be employed alone as the sample 1.

[0017]

The analysis plate 2 is made of silicon, for example, and includes a main surface 2a and a main surface 2b opposite to the main surface 2a. As illustrated in Figs. 1 and 2, a recess 2c is provided in the main surface 2b of the analysis plate 2. On a bottom surface 2ca of the recess 2c, a protrusion 2d which is spherical in shape and functions as a hemispherical SIL is formed. The surface of the protrusion 2d forms a locally spherical surface 2da. The recess 2c and the protrusion 2d are integrally formed by digging in the analysis plate 2 from the main surface 2b. Accordingly, the protrusion 2d functioning as an SIL does not protrude from a portion of the main surface 2b where the recess 2c is not provided. Fig. 4 is a plan view of the analysis plate 2 as viewed from the main surface 2b side.

[0018]

The sample 1 is mounted on the main surface 2a of the analysis plate 2 so that a main surface 1ab of the semiconductor substrate 1a is situated close to the analysis plate 2. At this time, the sample 1 is mounted on the analysis plate 2 in close contact therewith. Since both the analysis plate 2 and the semiconductor substrate 1a of the sample 1 are made of silicon, a center O of the locally spherical surface 2da of the protrusion 2d functioning as a hemispherical SIL is located on the main surface 1aa of the semiconductor substrate 1a provided on the analysis plate 2, as illustrated in Fig. 2. Respective thicknesses Tplate and Tsi of the analysis plate 2 and the semiconductor substrate 1a are determined to satisfy the following equation. In the following equation, R represents a radius of the locally spherical surface 2da of the protrusion 2d.

[0019]

[Equation 1]

5

10

15

20

[0020]

The SIL driver 10 includes the stage 11, the chuck 12 for supporting the stage 11 by engaging an edge portion of the stage 11, and a chuck driver 13 for moving the chuck 12. As illustrated in Fig. 2, the stage 11 includes a main surface 11a and a main surface 11b opposite to the main surface 11a, and is made of a material that transmits light, such as transparent quartz glass. On the main surface 11a of the stage 11, the analysis plate 2 is mounted with its main surface 2b situated close to the stage 11.

[0021]

5

10

15

20

25

The analysis plate 2 is also mounted on a top surface of the chuck 12 with its main surface 2b facing downward. The chuck 12, like the stage 11, is made of a material that transmits light, such as transparent quartz glass, and functions to fix the analysis plate 2 on the stage 11 by vacuum suction. More specifically, the chuck 12 has formed therein an exhaust hole 12a that opens into the top surface of the chuck 12, and the analysis plate 2 is mounted on the chuck 12 so as to block the opening of the exhaust hole 12a. Thus, discharging an air within the exhaust hole 12a to the outside of the chuck 12 will allow the analysis plate 2 to be attracted to the chuck 12 by vacuum suction. As a result, the analysis plate 2 is fixed on the stage 11.

[0022]

The chuck driver 13 is capable of moving the chuck 12 in parallel with the main surface 11a of the stage 11. Also, the chuck driver 13 is capable of moving the chuck 12 along a direction perpendicular to the main surface 11a of the stage 11. As the chuck 12 is moved, also the stage 11 is moved in the same manner because the stage 11 is supported by the chuck 12. Further, as the chuck 12 is moved, also the analysis plate 2 is moved in the same manner because the analysis plate 2 is fixed on the stage 11. Accordingly, when the chuck driver 13 moves the chuck 12 in parallel with the main

surface 11a of the stage 11, the analysis plate 2 is moved in parallel with the main surface 2a of the analysis plate 2. On the other hand, when the chuck driver 13 moves the chuck 12 along a direction perpendicular to the main surface 11a of the stage 11, the analysis plate 2 is moved along a direction perpendicular to the main surface 2a of the analysis plate 2.

[0023]

In this way, it is possible to move the analysis plate 2 in parallel with the main surface 2a and along a direction perpendicular to the main surface 2a by the action of the SIL driver 10.

10 [0024]

5

15

20

25

The prober 40 includes the probe card 41, a probe needle 42 connected to the probe card 41, and a probe driver 43. The probe card 41 and the probe needle 42 are situated above the sample 1 mounted on the analysis plate 2. The probe driver 43 is capable of moving the probe card 41 in parallel with the main surface 2a of the analysis plate 2, by which it becomes possible to move the probe needle 42 in parallel with the main surface 2a of the analysis plate 2. Also, the probe driver 43 is capable of moving the probe card 41 along a direction perpendicular to the main surface 2a of the analysis plate 2, by which it becomes possible to move the probe needle 42 along a direction perpendicular to the main surface 2a of the analysis plate 2. In back surface analysis, the probe driver 43 moves the probe card 41 to bring the probe needle 42 into contact with an electrode pad (not illustrated) provided in the device forming layer 1b of the sample 1.

[0025]

The tester 50 generates a test pattern required for failure analysis and sends the generated test pattern to the probe card 41. The probe card 41 applies the test pattern to the sample 1 via the probe needle 42, to thereby supply a predetermine electrical signal to

the sample 1.

5

10

15

20

25

[0026]

The failure detector 20 includes an optical microscope 21 which is provided with an optical system 21a including an objective lens and the like and a photodetector 21b, and a display 22. The optical microscope 21 is situated below the stage 11.

[0027]

The photodetector 21b of the optical microscope 21 is capable of detecting extremely feeble light which is measured in photon, and includes a photomultiplier tube, an image sensor, and the like. In operation, light 90 emitted from a spot of current leakage in the device forming layer 1b of the sample 1 passes through the semiconductor substrate 1a, the analysis plate 2, the stage 11 and the optical system 21a, to enter the photodetector 21b.

[0028]

The microscope driver 23 is capable of moving the optical microscope 21 in parallel with the main surface 2a of the analysis plate 2, and is also capable of moving the optical microscope 21 along a direction perpendicular to the main surface 2a of the analysis plate 2.

[0029]

The sample support jig 30 supports the sample 1 independently of the analysis plate 2 from above the top surface thereof by vacuum suction. The sample support jig 30 has an exhaust hole 30a formed therein, and is situated on an edge portion of the top surface of the sample 1 so that one end of the exhaust hole 30a is blocked by the sample 1. Thus, discharging an air within the exhaust hole 30a to the outside of the sample support jig 30 will allow the sample 1 to be attracted to the sample support jig 30 by vacuum suction.

[0030]

Out of the components of the failure analyzer 100 of the first embodiment, those other than the chuck driver 13, the display 22, the microscope driver 23, the probe driver 43 and the tester 50 are accommodated in one housing (not illustrated). The sample support jig 30 is attached to the housing, so that it is fixedly positioned in the housing. Accordingly, moving the analysis plate 2 or the probe needle 42 will not result in movement of the sample support jig 30 nor movement of the sample 1 held by the sample support jig 30.

[0031]

5

10

15

20

In the meantime, the chuck driver 13, the microscope driver 23, and the probe driver 43 move the chuck 12, the optical microscope 21, and the probe card 41, respectively, based on the same xyz-rectangular coordinate system. The XYZ-rectangular coordinate system is defined for example by the X and Y axes that extend in parallel with the main surface 2a of the analysis plate 2 and the main surface 11a of the stage 11 and by the Z axis that extends along a direction perpendicular to the X and Y axes. Then, respective values of X, Y, and Z coordinates in the XYZ-rectangular coordinate system are externally specified. The chuck driver 13, the microscope driver 23, and the probe driver 43 move the chuck 12, the optical microscope 21 and the probe card 41, respectively, to the positions specified. It is noted that this XYZ-rectangular coordinate system is hereinafter referred to as the "XYZ-rectangular coordinate system is hereinafter referred to as the "XYZ-rectangular coordinate system is hereinafter referred to as the "XYZ-rectangular coordinate system Q".

[0032]

Next, a method of carrying out emission analysis on the sample 1 using the failure analyzer 100 of the first embodiment is described.

25 [0033]

First, the sample 1 is mounted on the analysis plate 2 fixed on the stage 11 as described above. Then, the chuck 12 is moved along a direction perpendicular to the main surface 11a of the stage 11 by the chuck driver 13 to bring the sample 1 and the sample support jig 30 into contact with each other. As a result, the sample support jig 30 is situated on the top surface of the sample 1 so that one end of the exhaust hole 30a of the sample support jig 30 is blocked by the sample 1.

[0034]

5

10

15

Then, an air within the exhaust hole 30a is discharged out of the other end of the exhaust hole 30a to draw the sample 1 to the sample support jig 30 by suction force. As a result, the sample 1 is held by the sample support jig 30 while being in close contact with the analysis plate 2, and the sample 1 is fixedly positioned.

[0035]

Subsequently, the chuck 12 is moved in parallel with the main surface 11a of the stage 11 by the chuck driver 13 to move the analysis plate 2 in parallel with the main surface 2a of the analysis plate 2. Then, the movement of the chuck 12 is stopped when the protrusion 2d functioning as an SIL comes to a position just below a certain region of the semiconductor chip 1c that is being subjected to failure analysis.

[0036]

Thereafter, the optical microscope 21 is moved in parallel with the main surface 20 2a of the analysis plate 2 by the microscope driver 23 to situate the optical system 21a and the photodetector 21b just below the protrusion 2d of the analysis plate 2. Further, the optical microscope 21 is moved along a direction perpendicular to the main surface 2a of the analysis plate 2 by the microscope driver 23 so that the optical system 21a is situated at a predetermined distance from the protrusion 2d of the analysis plate 2.

[0037]

Next, the probe needle 42 is brought into contact with an electrode pad (not illustrated) provided in the semiconductor chip 1c, using the probe driver 43. Then, a predetermined test pattern is generated in the tester 50 and is sent to the probe card 41, which in turn applies the test pattern to the sample 1 via the probe needle 42. As a result, a predetermined electrical signal is applied to the sample 1, to place the sample 1 in an operating mode.

[0038]

5

10

15

20

25

Then, the light 90 which is emitted from a spot of current leakage in the device forming layer 1b of the semiconductor chip 1c is detected in the optical microscope 21 through the protrusion 2d of the analysis plate 2 and the stage 11. In the optical microscope 21, the input light 90 is converged in the optical system 21a and converted into a photoelectron by the photomultiplier tube of the photodetector 21b. Subsequently, the photoelectron is electrically multiplied by the photomultiplier tube, to be again converted into light, which then enters the image sensor. The image sensor outputs the emission position and the emission intensity of the light 90 to the display 22 as detection data. The display 22, based on the detection data from the image sensor of the photodetector 21b, displays the emission position and emission intensity of the light 90 emitted from the spot of current leakage as an emitted light image on a monitor (not illustrated). At that time, the display 22 also displays a pattern image of the sample 1 previously stored as data on the monitor. Thus, the pattern image and the emitted light image are displayed while overlapping each other.

[0039]

In the foregoing manner, a failure caused in the device forming layer 1b is detected in the failure detector 20 using the optical system 21a. In the first embodiment, as illustrated in Fig. 2, the center O of the locally spherical surface 2da of the protrusion

2d and an aplanatic point of the light 90 in the sample 1 are located at the same position. In other words, in the first embodiment, the aplanatic point is located on the main surface 1 aa of the semiconductor substrate 1a. Since the protrusion 2d functions as a hemispherical SIL, as illustrated in Fig. 2, the light 90 emitted from the spot of current leakage travels straightforward toward the optical system 21a without being refracted at the surface of the protrusion 2d.

[0040]

Next, failure analysis of the sample 1 is initiated based on the emitted light image and the pattern image displayed on the monitor of the display 22. More specifically, the location, type, or the like of the failure is specified based on the position, brightness, or the like of the emitted light image displayed on the monitor. This can lead to detection of a defect in an oxide film of the sample 1, a break in an interconnection line of the sample 1, or the like. Further, a functional failure of the sample 1 or the like caused due to current leakage can be detected also.

15 [0041]

5

10

20

25

After the completion of the failure analysis of the certain region of the semiconductor chip 1c, the probe card 41 is moved using the probe driver 43, to bring the probe needle 42 out of contact with the sample 1. Subsequently, the analysis plate 2 is moved in parallel with the main surface 2a thereof so that the protrusion 2d is situated just below a different region of the same semiconductor chip 1c. Then, failure analysis of the different region of the semiconductor chip 1c is carried out in the same manner as described above. At the completion of the failure analysis of the semiconductor chip 1c, the analysis plate 2 is moved to carry out failure analysis of another one of the semiconductor chips 1c.

[0042]

As described, the failure analyzer 100 of the first embodiment includes, aside from the sample 1, the analysis plate 2 which includes the protrusion 2d functioning as an SIL. Thus, the location of the protrusion 2d can be shifted relative to a target region for analysis in the device forming layer 1b of the sample 1. Accordingly, the range of analysis can be moved, which facilitates failure analysis of an arbitrary region.

[0043]

Further, since the protrusion 2d functioning as an SIL does not protrude from the main surface 2b of the analysis plate 2, it is possible to stably mount the sample 1 on the stage 11 with the analysis plate 2 interposed therebetween as in the first embodiment.

10 [0044]

5

15

20

25

Moreover, in the first embodiment, the sample 1 is held independently of the analysis plate 2 by the sample support jig 30. Hence, the sample 1 is not moved even when the analysis plate 2 is moved. Therefore, it is possible to easily align the protrusion 2d functioning as an SIL with a target region for analysis.

【0045】

It is noted that though the protrusion 2d of the analysis plate 2 is formed so as to function as a hemispherical SIL in the first embodiment, the protrusion 2d may alternatively be formed so as to function as a super-spherical SIL as illustrated in Fig. 5. In this case, the center O of the locally spherical surface 2da of the protrusion 2d is located at a position different from the position of the aplanatic point in the sample 1. Specifically, assuming that n is a refractive index of the semiconductor substrate 1a, the center O of the locally spherical surface 2da of the protrusion 2d is located at a distance of R/n along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a within the semiconductor substrate 1a. On the other hand, the aplanatic point is located on the main surface 1aa of the semiconductor substrate

- 1a. Since the protrusion 2d functions as a super-spherical SIL, the light 90 emitted from a spot of current leakage is refracted at the surface of the protrusion 2d as illustrated in Fig.
- 5. It is noted that in the case where the protrusion 2d functions as a super-spherical SIL, the respective thicknesses Tplate and Tsi of the analysis plate 2 and the semiconductor substrate 1a are determined to satisfy the following equation.

[0046]

[Equation 2]

5

10

15

20

25

Tplate + Tsi >
$$R(1+1/n)$$

[0047]

Though the above description of the first embodiment has been made about the failure analyzer 100 adapted to carry out emission analysis by way of example, the invention can also be applied to a failure analyzer for carrying out OBIC analysis or OBRCH analysis, and a failure analyzer for carrying out a laser voltage probing analysis. More specifically, OBIC analysis or OBRCH analysis can be accomplished by irradiating the sample 1 with laser light through the protrusion 2d of the analysis plate 2. And, laser voltage probing analysis can be accomplished by irradiating the sample 1 with laser light through the protrusion 2d of the analysis plate 2 and detecting reflected light from the sample 1 through the protrusion 2d. Below, a specific description is made about a case where the invention is applied to a failure analyzer for carrying out OBIC analysis as a representative example of application of the invention to a failure analyzer which carries out failure analysis utilizing irradiation of the sample 1 with light through the protrusion 2d of the analysis plate 2.

[0048]

Fig. 6 illustrates the structure of a failure analyzer 101 according to a modification of the first embodiment. The failure analyzer 101 is a failure analyzer for

carrying out OBIC analysis on the sample 1 and is different from the failure analyzer 100 illustrated in Fig. 1 in that a failure detector 25 is provided in place of the failure detector 20.

[0049]

5

10

20

25

The failure detector 25 includes an optical microscope 26 including an optical system 26a formed of an objective lens and the like and a laser light source 26b, a current detector 27 connected to the probe needle 42, and a display 28. The optical microscope 26 is situated below the stage 11. The microscope driver 23 is capable of moving the optical microscope 26 in parallel with the main surface 2a of the analysis plate 2 and is also capable of moving the optical microscope 26 along a direction perpendicular to the main surface 2a of the analysis plate 2. The other components included in the structure of the failure analyzer 101 are identical to those of the failure analyzer 100 illustrated in Fig. 1, and thus the description thereof is omitted.

[0050]

Next, a method of carrying out OBIC analysis on the sample 1 using the failure analyzer 101 is described.

[0051]

First, in the same manner as in the above-described method of carrying out emission analysis, the sample 1 is mounted on the analysis plate 2 fixed on the stage 11, and the analysis plate 2 is moved under control of the SIL driver 10 to bring the sample 1 and the sample support jig 30 into contact with each other. Then, the sample 1 is held by the sample support jig 30, to be fixedly positioned.

[0052]

Then, the analysis plate 2 is moved so that the protrusion 2d is situated just below a certain region of the semiconductor chip 1c that is being subjected to failure

analysis. Thereafter, the optical microscope 26 is moved using the microscope driver 23, to situate the optical system 26a and the laser light source 26b just below the protrusion 2d of the analysis plate 2. Further, the optical microscope 26 is moved along a direction perpendicular to the main surface 2a of the analysis plate 2 using the microscope driver 23 so that the optical system 26a is situated at a certain distance from the protrusion 2d of the analysis plate 2

[0053]

5

10

15

20

Then, the probe needle 42 is brought into contact with an electrode pad provided in the semiconductor chip 1c to apply a test pattern generated in the tester 50 to the sample 1 via the probe needle 42.

[0054]

Subsequently, the laser light source 26b is caused to generate laser light 91, which then enters the optical system 26a. The laser light 91 is converged in the optical system 26a and irradiates the device forming layer 1b of the sample 1 through the stage 11 and the protrusion 2d of the analysis plate 2. Upon irradiation of the sample 1 with the laser light 91, an optical beam induced current is generated in the device forming layer 1b and is supplied to the current detector 27 via the probe needle 42. The current detector 27 amplifies the received optical beam induced current, converts the current into luminance information, and inputs the current to the display 28. The display 28 displays an OBIC image on a monitor (not illustrated) based on the received luminance information. At this time, the display 28 also displays a pattern image of the sample 1 previously stored as data on the monitor. Thus, the pattern image and the OBIC image are displayed while overlapping each other, and a failure caused in the device forming layer 1b is detected by the failure detector 25.

[0055]

In this way, the invention can be applied not only to the case of detecting light emitted from the device forming layer 1b through the protrusion 2d, such as emission analysis, but also to the case of irradiating a light onto the device forming layer 1b through the protrusion 2d, such as OBIC analysis. It is noted that light which is emitted from the device forming layer 1b and is dealt with in emission analysis, light from the device forming layer 1b such as reflected light from the device forming layer 1b dealt with in laser voltage probing analysis, and light which irradiates the device forming layer 1b and is dealt with in OBIC analysis, OBIRCH analysis, and laser voltage probing analysis, may be hereinafter collectively referred to as "analysis light."

10 [0056]

5

15

20

25

Second Embodiment

Fig. 7 illustrates the structure of a failure analyzer 200 according to a second embodiment of the invention. The failure analyzer 200 of the second embodiment is different from the failure analyzer 100 of the first embodiment in that the analysis plate 2 is used as a stage for mounting the sample 1 in place of the stage 11, and that an SIL driver 210 is provided in place of the SIL driver 10. Fig. 7 illustrates sectional structures of the sample 1, the analysis plate 2, the sample support jig 30, the probe card 41, and a chuck 212 described later.

[0057]

The analysis plate 2 of the second embodiment not only functions to increase resolution by means of an SIL, but also is used as a stage for mounting the sample 1. Thus, the analysis plate 2 of the second embodiment is formed thicker than the aforementioned analysis plate 2 of the first embodiment in order to increase strength. The SIL driver 210 includes the chuck 212 for supporting the analysis plate 2 by engaging an edge portion of the analysis plate 2, and a chuck driver 213 for shifting the location of

the chuck 212. The sample 1 is mounted not only on the analysis plate 2 but also on the chuck 212.

[0058]

5

10

15

20

25

The chuck driver 213 is capable of moving the chuck 212 in parallel with the main surface 2a of the analysis plate 2 or along a direction perpendicular to the main surface 2a of the analysis plate 2, based on the XYZ-rectangular coordinate system Q. Thus, the analysis plate 2 can be moved in parallel with the main surface 2a thereof and along a direction perpendicular to the main surface 2a thereof, by the action of the SIL driver 210. The other components are identical to those of the failure analyzer 100 of the first embodiment, and thus the description thereof is omitted.

[0059]

Next, a method of carrying out emission analysis on the sample 1 using the failure analyzer 200 of the second embodiment is described in detail.

[0060]

First, the sample 1 is mounted on the main surface 2a of the analysis plate 2 supported by the chuck 212, and on the chuck 212. At that time, the sample 1 and the analysis plate 2 are brought into close contact with each other. Then, the chuck 212 is moved along a direction perpendicular to the main surface 2a of the analysis plate 2 using the chuck driver 213, to bring the sample 1 and the sample support jig 30 into contact with each other. Then, vacuum evacuation causes the sample 1 to be drawn to the sample support jig 30 by suction force. As a result, the sample 1 is held by the sample support jig 30 while being in close contact with the analysis plate 2, and the sample 1 is fixedly positioned.

[0061]

Subsequently, the chuck 212 is moved using the chuck driver 213, to move the

analysis plate 2 in parallel with the main surface 2a thereof. The movement of the chuck 212 is stopped when the protrusion 2d functioning as an SIL is situated just below a certain region of the semiconductor chip 1c that is being subjected to failure analysis. Thereafter, in the same manner as in the method described in the first embodiment, the optical microscope 21 is moved to a certain position by the microscope driver 23 and a test pattern generated by the tester 50 is applied to the sample 1.

[0062]

5

10

15

20

25

Then, the light 90 which is emitted from a spot of current leakage in the device forming layer 1b of the semiconductor chip 1c is detected in the optical microscope 21 through the protrusion 2d of the analysis plate 2. Then, the display 22 receives the result of detection from the optical microscope 21, and displays an emission position and an emission intensity of the light 90 emitted from the spot of current leakage as an emitted light image on a monitor (not illustrated), based on the result of detection. At that time, the display 22 also displays a pattern image of the sample 1 previously stored as data on the monitor. Thus, the pattern image and the emitted light image are displayed while overlapping each other, and a failure caused in the device forming layer 1b is detected in the failure detector 20. Then, failure analysis of the sample 1 is initiated based on the emitted light image and the pattern image displayed on the monitor of the display 22.

[0063]

As is made clear from the above description, in the failure analyzer 200 of the second embodiment, the analysis plate 2 including an SIL is also used as a stage for mounting the sample 1. Accordingly, unlike in the first embodiment, there is no need of additionally providing the stage 11 separately from the analysis plate 2. This allows for reduction of costs of the material of the failure analyzer 200 while ensuring that the sample 1 is stably mounted on a stage. Further, since reflection of analysis light at the

main surfaces 11a and 11b of the stage 11 does not occur, the light can be used more efficiently in back surface analysis.

[0064]

5

10

15

20

25

It is noted that though the analysis plate 2 of the second embodiment is made of silicon, it may alternatively be made of transparent quartz glass, for example. This case is equivalent to the case where a protrusion functioning as an SIL is formed in the main surface 11b of the stage 11 made of quartz glass which is used in the first embodiment and that stage 11 is used in place of the analysis plate 2 of the second embodiment.

[0065]

Fig. 8 is a partially enlarged view of the structure of the failure analyzer 200 when the analysis plate 2 of the second embodiment is made of quartz glass. Fig. 8 illustrates cross-sectional structures of the analysis plate 2 and the sample 1.

[0066]

When the analysis plate 2 is made of quartz glass, the analysis plate 2 and the semiconductor substrate 1a of the sample 1 are made of different materials. For this reason, the light 90 emitted from the device forming layer 1b is refracted at an interface between the semiconductor substrate 1a and the analysis plate 2. Accordingly, unlike the case where the analysis plate 2 and the semiconductor substrate 1a are made of the same material, it is necessary to locate the center O of the locally spherical surface 2da of the protrusion 2d functioning as a hemispherical SIL at a position different from the position of an aplanatic point. For example, under conditions that the thickness Tplate of the analysis plate 2 is $2000 \,\mu$ m, the thickness Tsi of the semiconductor substrate 1a is $300 \,\mu$ m, a refractive index provided by the analysis plate 2 made of quartz glass is 1.52, and a refractive index provided by the semiconductor substrate 1a made of silicon is 3.5, the radius R of the locally spherical surface 2da of the protrusion 2d is set to $1675 \,\mu$ m and

the center O of the locally spherical surface 2da of the protrusion 2d is located at a distance of 185μ m along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a toward the inside of the semiconductor substrate 1a.

[0067]

5

10

15

20

25

Also in the case where the analysis plate 2 made of quartz glass is provided with the protrusion 2d of functioning as a superspherical SIL, as illustrated in Fig. 9, the light 90 emitted from the device forming layer 1b is refracted at the interface between the semiconductor substrate 1a and the analysis plate 2. Hence, unlike in the case where the analysis plate 2 and the semiconductor substrate 1a are made of the same material, the center O of the locally spherical surface 2da of the protrusion 2d functioning as a superspherical SIL is not located at a position which is at a distance of R/n along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a toward the inside of the semiconductor substrate 1a.

[0068]

For example, under conditions that the thickness Tplate of the analysis plate 2 is $2000 \,\mu$ m, the thickness Tsi of the semiconductor substrate 1a is $300 \,\mu$ m, a refractive index provided by the analysis plate 2 made of quartz glass is 1.52, and a refractive index provided by the semiconductor substrate 1a made of silicon is 3.5, the radius R of the locally spherical surface 2da of the protrusion 2d is set to $1145 \,\mu$ m and the center O of the locally spherical surface 2da of the protrusion 2d is located at a distance of $930 \,\mu$ m along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a toward the inside of the semiconductor substrate 1a. When both the analysis plate 2 and the semiconductor substrate 1a are made of silicon under the same conditions as noted above, the center O of the locally spherical surface 2da of the

protrusion 2d is located at a distance of 327 μ m (approximately equal to 1145 μ m /3.5) along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a toward the inside of the semiconductor substrate 1a.

[0069]

5

10

15

25

Thus, the analysis plate 2 made of quartz glass provides a lower refractive index than the analysis plate 2 made of silicon. Hence, while the effects of increasing resolution produced by an SIL may be lessened, analysis light can be more efficiently used in back surface analysis because quartz glass transmits light with higher transmittance than silicon.

[0070]

Third Embodiment

Fig. 10 illustrates the structure of a failure analyzer 300 according to a third embodiment of the invention. Fig. 11 is a partial enlarged view of the structure illustrated in Fig. 10. Major differences of the failure analyzer 300 of the third embodiment from the failure analyzer 100 of the first embodiment lie in that an SIL 60 functioning as a hemispherical SIL is provided in place of the analysis plate 2 and an SIL driver 310 and the stage 11 are provided in place of the SIL driver 10. In Figs. 10 and 11, the sample 1, the SIL 60, the sample support jig 30, the stage 11, the probe card 41, and a chuck 312 later described, are illustrated in section.

20 [0071]

The SIL 60 is spherical in shape and is made of silicon, for example. A surface of the SIL 60 includes a flat region 60a and a locally spherical region 60b extending continuously with the flat region 60a. The SIL 60 is embedded in the stage 11 with the locally spherical region 60b facing the main surface 11b of the stage 11. The flat region 60a of the surface of the SIL 60 is flat as well as the main surface 11a of the

stage 11 and is exposed from the main surface 11a of the stage 11.

[0072]

5

15

20

25

The sample 1 is mounted on the main surface 11a of the stage 11 and on the flat region 60a of the SIL 60 so that the main surface 1ab of the semiconductor substrate 1a is situated close to the stage 11. At that time, the SIL 60 and the sample 1 are brought into close contact with each other. Then, a center O of the locally spherical region 60b of the SIL 60 is located on the main surface 1aa of the semiconductor substrate 1a mounted on the stage 11 as illustrated in Fig. 11.

[0073]

The SIL driver 310 includes the chuck 312 for supporting the stage 11 with the SIL 60 embedded therein by engaging an edge portion of the stage 11, and a chuck driver 313 for shifting the location of the chuck 312. The sample 1 is mounted not only on the stage 11 and the SIL 60 but also on the chuck 312.

[0074]

The chuck driver 313 is capable of moving the chuck 312 in parallel with the main surface 11a of the stage 11 and in a direction perpendicular to the main surface 11a of the stage 11, based on the XYZ-rectangular coordinate system Q. Thus, the stage 11 and the SIL 60 can be moved in parallel with the main surface 11a of the stage 11 by the action of the SIL driver 310 and along a direction perpendicular to the main surface 11a. Further, the sample support jig 30 of the third embodiment supports the sample 1 independently of the stage 11 and the chuck 312 from above the top surface thereof by vacuum suction. The other components of the structure are identical to those of the failure analyzer 100 of the first embodiment, and thus the description thereof is omitted.

[0075]

Next, a method of carrying out emission analysis on the sample 1 using the

failure analyzer 300 of the third embodiment is described.

[0076]

5

10

15

20

25

First, the sample 1 is mounted on the main surface 11a of the stage 11, the flat region 60a of the SIL 60 embedded in the stage 11, and the chuck 312. At that time, the sample 1 and the stage 11 are brought into close contact with each other. Then, the chuck 312 is moved along a direction perpendicular to the main surface 11a of the stage 11 using the chuck driver 313, to bring the sample 1 and the sample support jig 30 into contact with each other. Subsequently, vacuum evacuation causes the sample 1 to be drawn to the sample support jig 30 by suction force. As a result, the sample 1 is held by the sample support jig 30 while being in close contact with the SIL 60, and the sample 1 is fixedly positioned.

[0077]

Subsequently, the chuck 312 is moved using the chuck driver 313, to move the stage 11 in parallel with the main surface 11a thereof. The movement of the chuck 312 is stopped when the SIL 60 is situated just below a certain region of the semiconductor chip 1c that is being subjected to failure analysis. Thereafter, in the same manner as in the analysis method described in the first embodiment, the optical microscope 21 is moved to a certain position using the microscope driver 23 and a test pattern generated by the tester 50 is applied to the sample 1.

[0078]

Then, the light 90 which is emitted from a spot of current leakage in the device forming layer 1b of the semiconductor chip 1c is detected in the optical microscope 21 through the SIL 60 and the stage 11. The display 22 receives the result of detection from the optical microscope 21 and displays the emission position and the emission intensity of the light 90 emitted from the spot of current leakage as an emitted light image on a

monitor (not illustrated), based on the result of the detection. At that time, the display 22 also displays a pattern image of the sample 1 previously stored as data on the monitor. Thus, the pattern image and the emitted light image are displayed while overlapping each other, and a failure caused in the device forming layer 1b is detected in the failure detector 20. Then, failure analysis of the sample 1 is initiated based on the emitted light image and the pattern image displayed on the monitor of the display 22.

[0079]

5

10

15

20

After the completion of the failure analysis of the certain region of the semiconductor chip 1c, the probe card 41 is moved using the probe driver 43 so as to bring the probe needle 42 out of contact with the sample 1. Subsequently, the stage 11 is moved in parallel with the main surface 2a thereof, so that the SIL 60 is situated just below a different certain region of the same semiconductor chip 1c. Then, failure analysis of that region is carried out in the same manner as described above. After the completion of the failure analysis of one semiconductor chip 1c, the stage 11 is moved for failure analysis of another one of the semiconductor chips 1c.

[0080]

As described, since in the failure analyzer 300 of the third embodiment, the SIL 60 is embedded in the stage, it is possible to shift the location of the SIL 60 relative to a target region for analysis in the device forming layer 1b. Accordingly, the range of analysis can be moved, which facilitates failure analysis of an arbitrary region.

[0081]

Further, since the exposed surface of the SIL 60 from the stage 11, i.e., the flat region 60a, is flat as well as the main surface 11a of the stage 11, the sample 1 can be stably mounted on the stage 11 and the SIL 60.

25 [0082]

Moreover, in the third embodiment, the sample 1 is held independently of the stage 11 and the SIL 60 by the sample support jig 30. Hence, the sample 1 is not moved even when the stage 11 is moved. Therefore, it is possible to easily align the SIL 60 with a target region for analysis.

【0083】

5

20

25

Furthermore, since, in the third embodiment, the stage 11 is made of quartz glass, the range of analysis can efficiently be searched out even with the SIL 60 being embedded in the stage 11.

[0084]

While the SIL 60 is a hemispherical SIL, it may alternatively be a super-spherical SIL as illustrated in Fig. 12. In this case, assuming that a radius of the locally spherical region 60b of the SIL 60 is R, the center O of the locally spherical region 60b is located at a distance of R/n along the thickness of the semiconductor substrate 1a from the main surface 1aa of the semiconductor substrate 1a on the stage 11 toward the inside of the semiconductor substrate 1a, and the aplanatic point is located on the main surface 1aa of the semiconductor substrate 1a.

[0085]

Further, while the main surface 11b of the stage 11 is flat in Fig. 10, by performing some processes on a portion of the main surface 11a as illustrated in Fig. 13, a protrusion 11c functioning as a convex lens may be formed in alignment with the SIL 60 along the thickness of the stage 11 in the main surface 11b of the stage 11.

[0086]

In this case, back surface analysis is accomplished by either irradiating the device forming layer 1b with light through the protrusion 11c, the stage 11 and the SIL 60, or detecting light emitted from the device forming layer 1b through the SIL 60, the stage

11 and the protrusion 11c.

[0087]

Such additional provision of the protrusion 11c functioning as a convex lens in the main surface 11b of the stage 11 can increase the half converging angle θ , which provides for further improvement in resolution.

[0088]

5

10

15

20

25

Fourth Embodiment

Fig. 14 is a plan view of the analysis plate 2 according to a fourth embodiment of the invention as viewed from its main surface 2b side. As illustrated in Fig. 14, the analysis plate 2 of the fourth embodiment includes a plurality of recesses 2c provided in the main surface 2b, and protrusions 2d functioning as SILs provided on the bottom surfaces 2ca of the recesses 2c. The recesses 2c and the protrusions 2d are provided for the semiconductor chips 1c of the sample 1 and located in correspondence with the locations of the semiconductor chips 1c. Accordingly, when the sample 1 is mounted on the main surface 2a of the analysis plate 2, the recesses 2c and the protrusions 2d are situated below the semiconductor chips 1c of the sample 1.

[0089]

As described, since the analysis plate 2 of the fourth embodiment is provided with the plurality of recesses 2c and the plurality of protrusions 2d, the use of the analysis plate 2 of the fourth embodiment in place of the analysis plate 2 of the first or second embodiment can reduce a distance of relative movement between the sample 1 and the protrusion 2d in situating the protrusion 2d just below the semiconductor chip 1c that is being subjected to analysis. As a result, efficiency in failure analysis can be enhanced.

[0090]

Further, in the analysis plate 2 of the fourth embodiment, the plurality of

recesses 2c and the plurality of protrusions 2d are provided for the semiconductor chips 1c of the sample 1 and located in correspondence with the locations of the semiconductor chips 1c. Thus, employing the analysis plate 2 of the fourth embodiment in place of the analysis plate 2 of the first or second embodiment allows the sample 1 and the protrusion 2d to be moved relative to each other only within an area of one chip. Hence, efficiency in failure analysis can be further enhanced.

[0091]

5

10

15

20

25

While the fourth embodiment has described the case where the analysis plate 2 of the first or second embodiment is provided with the plurality of protrusions 2d, a plurality of SILs 60 may be embedded in the stage 11 of the third embodiment. Fig. 15 is a plan view of the stage 11 with the plurality of SILs 60 embedded therein as viewed from the main surface 11a side. As illustrated in Fig. 15, the plurality of SILs 60 embedded in the stage 11 are provided for the semiconductor chips 1c and located in correspondence with the locations of the semiconductor chips 1c.

[0092]

Such employment of the stage 11 with the plurality of SILs 60 embedded therein in place of the stage 11 of the aforementioned third embodiment can reduce the distance of the relative movement between the sample 1 and the SIL 60 when the SIL 60 is moved just below the semiconductor chip 1c to be analyzed. As a result, efficiency in failure analysis can be enhanced.

[0093]

Further, by employing, in place of the stage 11 of the aforementioned third embodiment, the stage 11 provided with the SILs 60 which are provided for the semiconductor chips 1c of the sample 1 and are located in correspondence with the locations of the semiconductor chips 1c, the range of the relative movement between the

sample 1 and the SIL 60 can be limited within an area of one chip. Hence, efficiency in failure analysis can be further enhanced.

[0094]

5

10

15

20

25

Fifth Embodiment

Figs. 16 and 17 are partial enlarged views of the structure of a failure analyzer according to a fifth embodiment of the invention. The failure analyzer of the fifth embodiment is different from the failure analyzer 100 of the first embodiment in that a plurality of recesses 2c is provided in the main surface 2b of the analysis plate 2, with each of the recesses 2c having the protrusion 2d provided on the bottom surface 2ca thereof, and that the locally spherical surfaces 2da of the protrusions 2d have different radiuses. Figs. 16 and 17 illustrate cross-sectional structures of the sample 1, the analysis plate 2, and the stage 11.

[0095]

As illustrated in Fig. 16, for example the protrusions 2d including the locally spherical surfaces 2da with a radius R1 and the protrusions 2d including the locally spherical surfaces 2da with a radius R2 smaller than the radius R1 are provided on the bottom surfaces 2ca of the recesses 2c of the analysis plate 2.

[0096]

As described above, when the protrusions 2d function as hemispherical SILs, the location of the aplanatic point in the sample 1 coincides with the location of the center O of the locally spherical surfaces 2da of the protrusions 2d. When the protrusions 2d function as super-spherical SILs, the aplanatic point is located at a distance of R/n from the center O of the locally spherical surfaces 2da of the protrusions 2d. Accordingly, the location of the aplanatic point observed in analysis carrying out using the protrusions 2d including the locally spherical surfaces 2da with the radius R1 is different from the

location of the aplanatic point observed in analysis carrying out using the protrusions 2d including the locally spherical surfaces 2da with the radius R2.

[0097]

Thus, as illustrated in Fig. 16, the protrusions 2d including the locally spherical surfaces 2da with the radius R1 can be used for failure analysis of the sample 1 whose semiconductor substrate 1a is great in thickness, and as illustrated in Fig. 17, the protrusions 2d including the locally spherical surfaces 2da with the radius R2 can be used for failure analysis of the sample 1 whose semiconductor substrate 1a is small in thickness.

10 [0098]

5

15

20

25

As described, in the failure analyzer of the fifth embodiment, the analysis plate 2 is provided with the plurality of protrusions 2d including the locally spherical surfaces 2da with different radiuses R. Hence, with only one analysis plate 2, it is possible to analyze a plurality of samples with different thicknesses. This improves efficiency in analysis.

[0099]

While in the fifth embodiment, the analysis plate 2 of the first embodiment is provided with the plurality of protrusions 2d including the locally spherical surfaces 2da with different radiuses R, the analysis plate 2 of the second embodiment may also be provided with the plurality of protrusions 2d including the locally spherical surfaces 2da with different radiuses R. This case also produces the same effects as noted above.

[0100]

Further, as illustrated in Fig. 18, a plurality of SILs 60 including the locally spherical regions 60b with different radiuses may be embedded in the stage 11 of the third embodiment. In this case, the use of only one stage 11 makes possible the analysis of a

plurality of samples with different thicknesses, thereby improving efficiency in analysis.

[0101]

5

15

20

25

Sixth Embodiment

Fig. 19 illustrates the structure of a failure analyzer 600 according to a sixth embodiment of the invention. The failure analyzer 600 of the sixth embodiment is different from the failure analyzer 100 of the aforementioned first embodiment in that an SIL driver 610 and a microscope driver 623 are provided in place of the SIL driver 10 and the microscope driver 23, respectively.

[0102]

As illustrated in Fig. 19, the SIL driver 610 includes the stage 11 and the chuck 12 which are also included in the failure analyzer 100 of the first embodiment, and further includes a chuck driver 613. The chuck driver 613 has the function of notifying the microscope driver 623 of movement information my of the chuck 12, in addition to the functions of the chuck driver 13 described in the first embodiment.

[0103]

As described in the first embodiment, in order to move the range of analysis, the chuck 12 is moved in parallel with the main surface 11a of the stage 11. The chuck driver 613 notifies the microscope driver 623 of the movement information mv of the chuck 12 at that time. Since the analysis plate 2 is fixed on the stage 11 as described above and the stage 11 is further supported by the chuck 12, the movement information mv notified by the chuck driver 613 can also be movement information of the analysis plate 2. The movement information mv includes, for example, the values of X and Y coordinates in the aforementioned XYZ-rectangular coordinate system Q.

[0104]

The microscope driver 623 moves the optical microscope 21 in parallel with the

main surface 2a of the analysis plate 2 based on the received movement information mv, so that the optical system 21a is situated just below the protrusion 2d.

[0105]

5

10

15

20

As described, in the failure analyzer 600 of the sixth embodiment, the chuck driver 613 notifies the microscope driver 623 of the movement information mv which can also be movement information of the analysis plate 2, and the microscope driver 623 moves the optical microscope 21 based on the received movement information mv. Accordingly, it is possible to automatically shift the optical system 21a and the photodetector 21b to appropriate locations in association with the movement of the analysis plate 2. As a result, the range of analysis can be more efficiently moved, which thereby shortens the time required for analysis.

[0106]

While in the sixth embodiment, the chuck driver 13 of the first embodiment has the additional function of notifying the microscope driver 23 of the movement information mv of the chuck 12, and the microscope driver 23 has the additional function of moving the optical microscope 21 based on the received movement information mv, the chuck driver 13 and the microscope driver 23 of the fifth embodiment may have the same additional functions as noted above. As another alternative, the chuck driver 213 of the second embodiment may have the additional function of notifying the microscope driver 23 of the movement information mv of the chuck 212, and the microscope driver 23 may have the additional function of moving the optical microscope 21 based on the received movement information mv. Those cases also produce the same effects as described above.

[0107]

As still another alternative, the chuck driver 313 of the third embodiment may

have the additional function of notifying the microscope driver 23 of the movement information mv of the chuck 312, and the microscope driver 23 may have the additional function of moving the optical microscope 21 based on the received movement information mv. In this case, it is possible to automatically move the optical system 21a and the photodetector 21b to appropriate positions in accordance with movement of the SIL 60. As a result, the range of analysis can be more efficiently moved, which thereby shortens the time required for analysis.

[0108]

5

10

15

20

25

Moreover, the effects described in the fourth embodiment can be produced by employing the analysis plate 2 of the fourth embodiment illustrated in Fig. 14, in place of the analysis plate 2 illustrated in Fig. 19.

[0109]

Seventh Embodiment

Fig. 20 illustrates the structure of a failure analyzer 700 according to a seventh embodiment of the invention. The failure analyzer 700 of the seventh embodiment is different from the failure analyzer 100 of the first embodiment in that a prober 740 including the sample support jig 30 is provided in place of the prober 40.

[0110]

The prober 740 includes the probe card 41 and the probe needle 42 which are also included in the failure analyzer 100 of the first embodiment, and further includes a probe/sample driver 745. The probe/sample driver 745 includes a supporting mechanism driver 743, a supporting mechanism 744 and the sample support jig 30 of the first embodiment.

[0111]

While, in the aforementioned first embodiment, the sample support jig 30 is

attached to the housing which contains the stage 11 and the like as described above, the sample support jig 30 of the seventh embodiment is attached to the supporting mechanism 744. Also the probe card 41 is attached to the supporting mechanism 744.

[0112]

5

20

25

The supporting mechanism driver 743 is capable of moving the supporting mechanism 744 in parallel with the main surface 2a of the analysis plate 2 or along a direction perpendicular to the main surface 2a of the analysis plate 2 based on the XYZ-rectangular coordinate system Q.

[0113]

Here, the sample support jig 30 and the probe card 41 are attached to the supporting mechanism 744 as described above. Also, the sample 1 is supported by the sample support jig 30 and the probe needle 42 is attached to the probe card 41. Accordingly, when the supporting mechanism 744 is moved with the sample 1 being supported by the sample support jig 30, the probe needle 42 and the sample 1 are moved while maintaining their positional relationship.

[0114]

In this way, by the action of the probe/sample driver 745, the sample 1 and the probe needle 42 can be moved in parallel with the main surface 2a of the analysis plate 2 while maintaining positional relationship therebetween, and along a direction perpendicular to the main surface 2a. The other components of the structure are identical to those of the failure analyzer 100 of the first embodiment, and thus the description thereof is omitted.

[0115]

Next, a method of carrying out emission analysis on the sample 1 using the failure analyzer 700 of the seventh embodiment is described.

[0116]

First, as described in the first embodiment, the sample 1 is mounted on the analysis plate 2 fixed on the stage 11. Then, the chuck 12 is moved along a direction perpendicular to the main surface 11a of the stage 11 using the chuck driver 13, to bring the sample 1 and the sample support jig 30 into contact with each other and thereby to cause vacuum suction to draw the sample 1 to the sample support jig 30. At that time, the probe needle 42 comes into contact with an electrode pad provided in the device forming layer 1b of the sample 1.

[0117]

5

10

15

20

25

Next, with the sample 1 and the analysis plate 2 in close contact with each other, the supporting mechanism 744 is moved in parallel with the main surface 2a of the analysis plate 2 using the supporting mechanism driver 743, so that a certain region of the semiconductor chip 1c to be analyzed is situated above the protrusion 2d. At this time, the sample 1 and the probe needle 42 are moved while maintaining their positional relationship. Then, the optical microscope 21 is moved to a certain position using the microscope driver 23, and a test pattern generated by the tester 50 is applied to the sample 1 via the probe needle 42.

[0118]

Then, the light 90 emitted from a spot of current leakage in the device forming layer 1b of the one semiconductor chip 1c is detected in the optical microscope 21 through the protrusion 2d of the analysis plate 2 and the stage 11, and failure analysis is initiated.

[0119]

After the completion of the failure analysis of the certain region of the semiconductor chip 1c, the supporting mechanism 744 is moved in parallel with the main surface 2a of the analysis plate 2 using the supporting mechanism driver 743, to move the

sample 1 so that the protrusion 2d is situated below a different region of the same semiconductor chip 1c. At this time, the probe needle 42 is also moved while maintaining its positional relationship with the sample 1. Then, in the same manner as described above, failure analysis of that region is carried out.

[0120]

5

10

15

20

25

As described, in the failure analyzer 700 of the seventh embodiment, the probe needle 42 and the sample 1 can be moved while maintaining their positional relationship. Accordingly, there is no need of moving the analysis plate 2 and the optical system 21a in order to move the range of analysis. This provides for improvement of efficiency in analysis.

[0121]

While the seventh embodiment has been made about a case where the prober 740 including the sample support jig 30 is used in place of the prober 40 of the first embodiment, the prober 740 including the sample support jig 30 may be used in place of the prober 40 of the second, third or fifth embodiment. This case also produces the same effects as noted above.

[0122]

Further, the same effects as described in the fourth embodiment can also be achieved by using the analysis plate 2 of the fourth embodiment illustrated in Fig. 14 in place of the analysis plate 2 illustrated in Fig. 20.

[0123]

[Advantageous Effect of the Invention]

In the first failure analyzer of the invention, because the analysis plate which includes the protrusion functioning as a solid immersion lens is provided separately from the sample, it is possible to shift the location of the protrusion relative to a failure site in a

device forming layer. Accordingly, the range of analysis can be moved, and failure analysis of an arbitrary portion can be easily carried out.

[0124]

Further, since the protrusion functioning as a solid immersion lens does not protrude from the second main surface of the analysis plate, it is possible to stably mount the sample on a stage with the analysis plate interposed therebetween.

[0125]

5

10

15

In the second failure analyzer of the invention, since the solid immersion lens is embedded in the stage, it is possible to shift the location of the solid immersion lens relative to a device forming layer. Accordingly, the range of analysis can be moved, and failure analysis of an arbitrary portion can be easily carried out.

[0126]

Further, since the surface of the solid immersion lens exposed from the stage is flat as well as the first main surface of the stage, it is possible to stably mount the sample on the stage and on the solid immersion lens.

[Brief Description of the Drawings]

- [Fig. 1] is a view showing the structure of a failure analyzer of a first embodiment of the invention.
- [Fig. 2] is a view showing the structure of the failure analyzer of the first embodiment of the invention.
 - [Fig. 3] is a plan view of a sample 1 which is a target of analysis.
 - [Fig. 4] is a plan view of an analysis plate of the first embodiment of the invention.
- [Fig. 5] is a view showing the structure of the failure analyzer of the first embodiment of the invention.

- [Fig. 6] is a view showing the structure of a variation of the failure analyzer of the first embodiment of the invention.
- [Fig. 7] is a view showing a structure of a failure analyzer of a second embodiment of the invention.
- 5 [Fig. 8] is a view showing the structure of the failure analyzer of the second embodiment of the invention.
 - [Fig. 9] is a view showing the structure of the failure analyzer of the second embodiment of the invention.
- (Fig. 10) is a view showing the structure of a failure analyzer of a third embodiment of the invention.
 - [Fig. 11] is a view showing the structure of the failure analyzer of the third embodiment of the invention.
 - [Fig. 12] is a view showing the structure of the failure analyzer of the third embodiment of the invention.
- 15 [Fig. 13] is a view showing the structure of the failure analyzer of the third embodiment of the invention.
 - [Fig. 14] is a plan view of an analysis plate of a fourth embodiment of the invention.
 - [Fig. 15] is a plan view of a stage of the fourth embodiment of the invention.
- [Fig. 16] is a view showing the structure of a failure analyzer of a fifth embodiment of the invention.
 - [Fig. 17] is a view showing the structure of the failure analyzer of the fifth embodiment of the invention.
- (Fig. 18) is a view showing the structure of the failure analyzer of the fifth embodiment of the invention.

(Fig. 19) is a view showing the structure of a failure analyzer of a sixth embodiment of the invention.

[Fig. 20] is a view showing the structure of a failure analyzer of a seventh embodiment of the invention.

[Explanation of Referenced Numerals]

5

10

1: sample; 1a: semiconductor substrate; 1aa, 1ab, 2a, 2b, 11a, 11b: main surfaces; 1b device forming layer; 1c: semiconductor chips, 2: analysis plate; 2c: recess: 2ca: bottom surface; 2d: protrusion; 2da: locally spherical surface; 10, 210, 310, 610: SIL driver; 11: stage; 11c: protrusion; 20, 25: failure detector; 21a, 26a: optical system; 30: sample support jig; 40, 740: prober; 42: probe needle; 60: solid immersion lens; 60a: flat region; 60b: locally spherical region; 90: light; 91: laser; 100, 101, 200, 300, 600, 700: failure analyzer; 745: probe/sample driver.

[Document Name] Abstract

[Abstract]

5

10

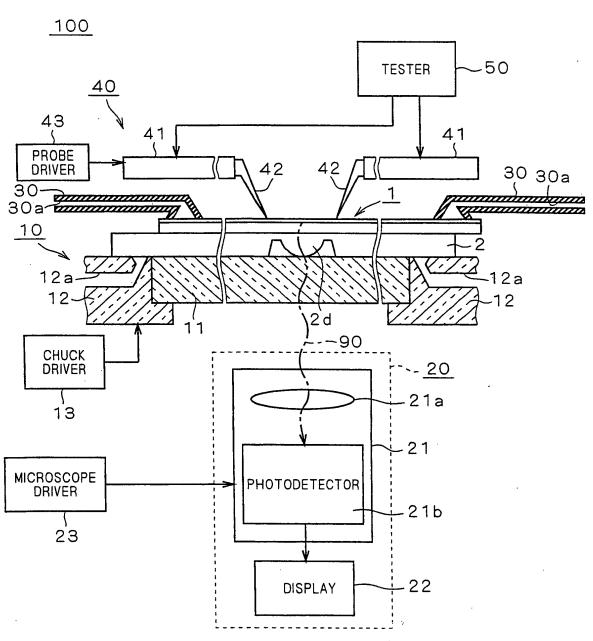
[Problems to be Solved] A failure analysis technique is provided, which is capable of stably mounting a sample on a stage and moving the range of analysis.

[Means to Solve the Problems] A sample 1 is mounted on a stage 11 with an analysis plate 2 interposed therebetween. A recess 2c is provided in a main surface 2b of the analysis plate 2, and a protrusion 2d functioning as a solid immersion lens is provided on a bottom surface 2ca of the recess 2c. The protrusion 2d does not protrude from the main surface 2b of the analysis plate 2. Because the analysis plate 2 which includes a solid immersion lens is provided separately from the sample 1, the range of analysis can be moved. Further, since the protrusion 2d does not protrude from the main surface 2b of the analysis plate 2, the sample 1 can be stably mounted on the stage 11 with the analysis plate 2 interposed therebetween.

[Selected Figure] Fig. 2



F I G . 1



1: SAMPLE

2: ANALYSIS PLATE

2d: PROTRUSION

10: SIL DRIVER

11: STAGE

20: FAILURE DETECTOR

21a: OPTICAL SYSTEM

30: SAMPLE SUPPORT JIG

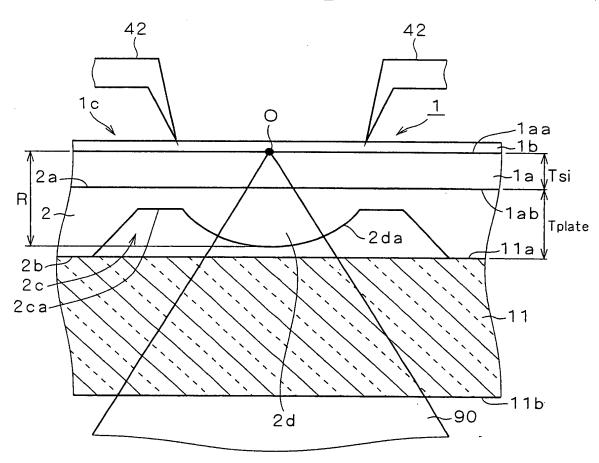
40: PROBER

42: PROBE NEEDLE

90: LIGHT

100: FAILURE ANALYZER

F 1 G . 2



1a: SEMICONDUCTOR SUBSTRATE

1b: DEVICE FORMING LAYER

1c: SEMICONDUCTOR CHIP

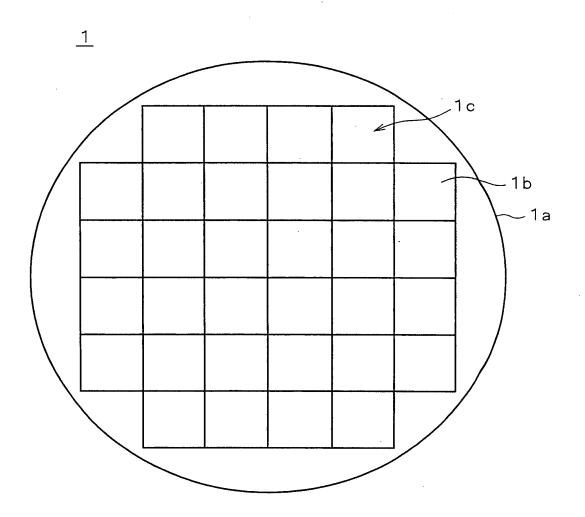
1aa, 1ab, 2a, 2b, 11a, 11b: MAIN SURFACES

2c: RECESS

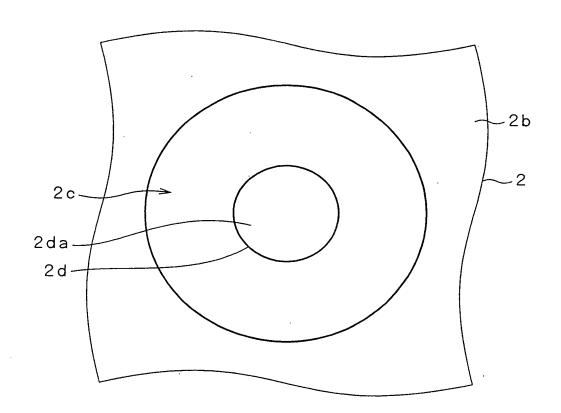
2ca: BOTTOM SURFACE

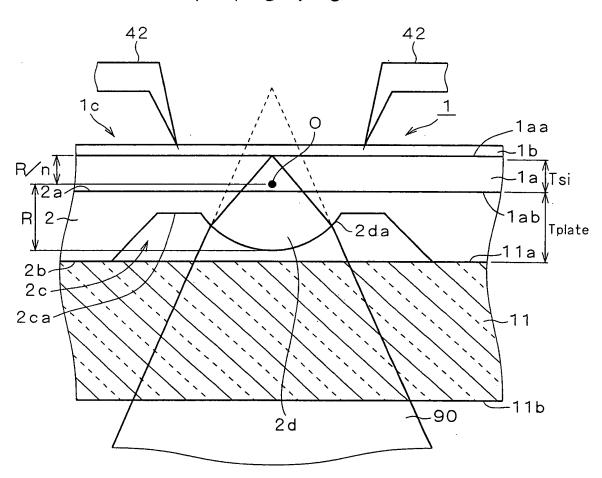
2da: LOCALLY SPHERICAL SURFACE

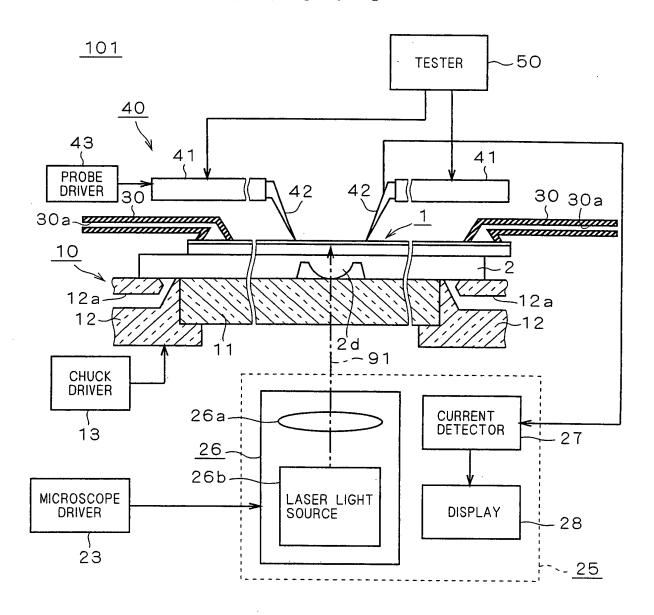
F I G . 3



F I G . 4





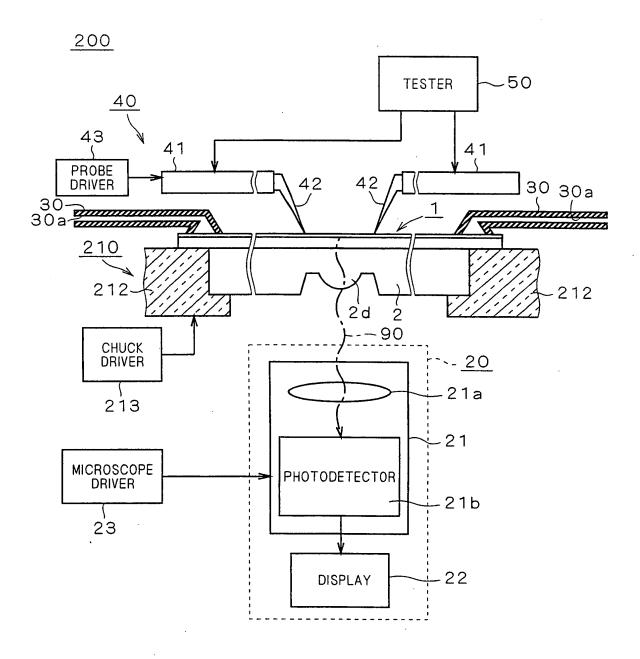


25: FAILURE DETECTOR

26a: OPTICAL SYSTEM

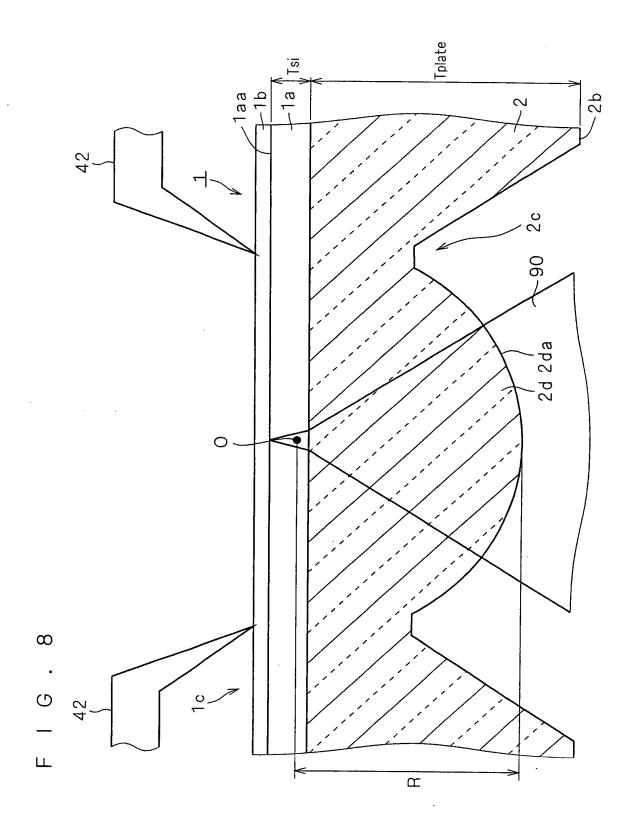
91:LASER

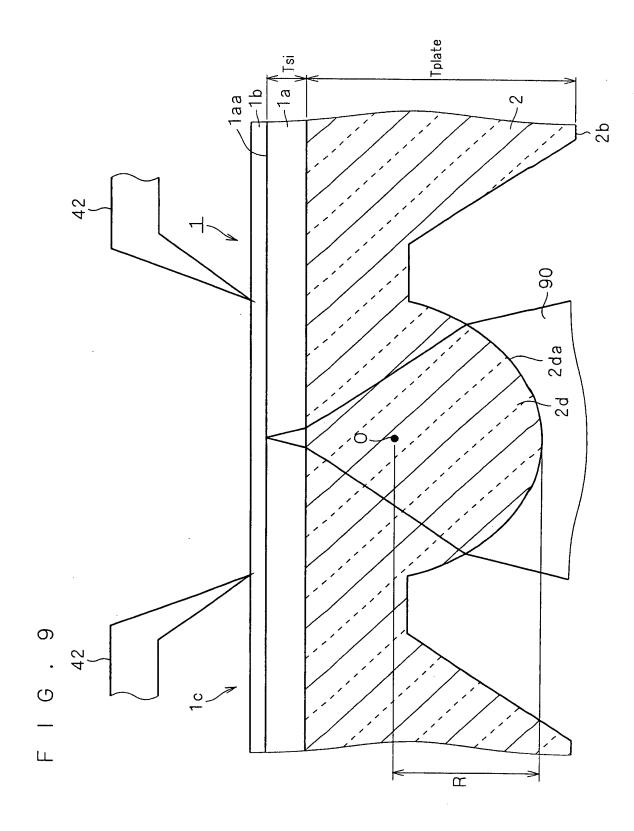
101: FAILURE ANALYZER

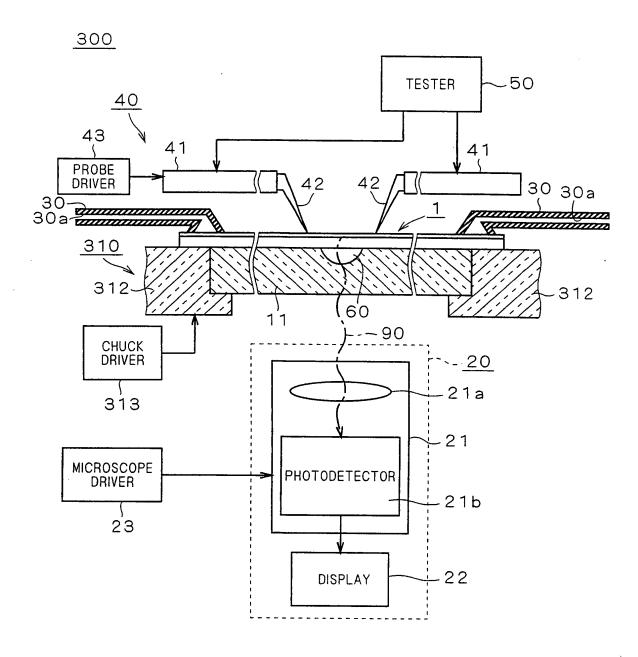


200: FAILURE ANALYZER

210: SIL DRIVER



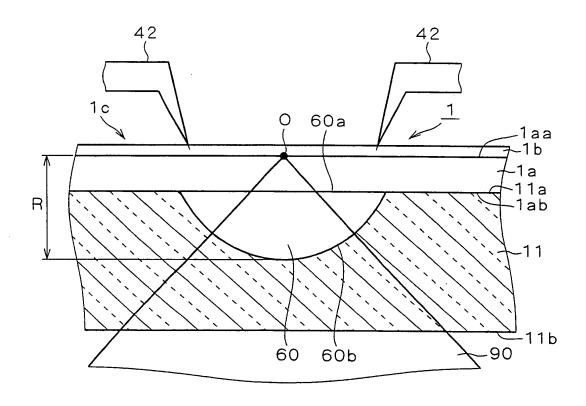




60: SOLID IMMERSION LENS

300: FAILURE ANALYZER

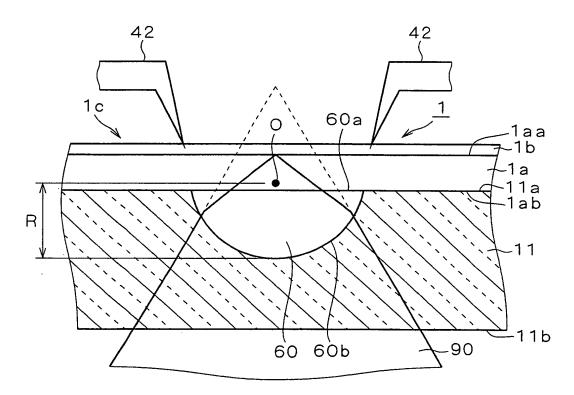
310: SIL DRIVER

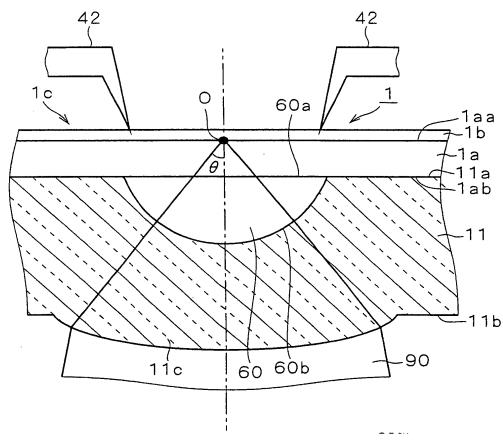


60a: FLAT REGION

60b: LOCALLY SPHERICAL REGION

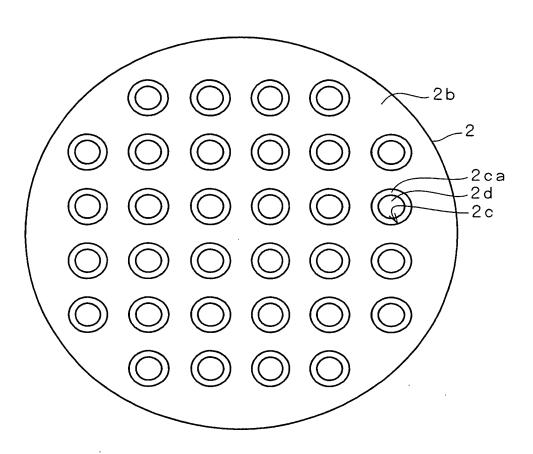
F I G . 1 2



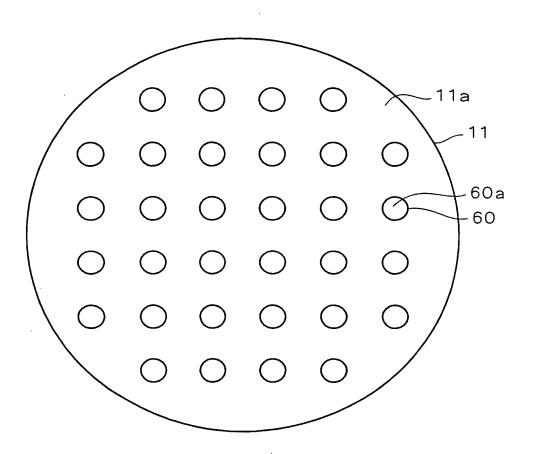


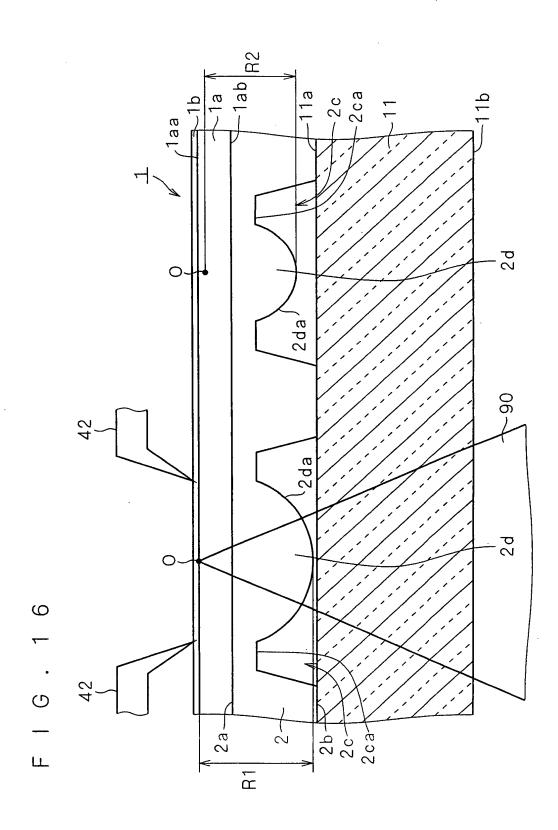
11c: PROTRUSION

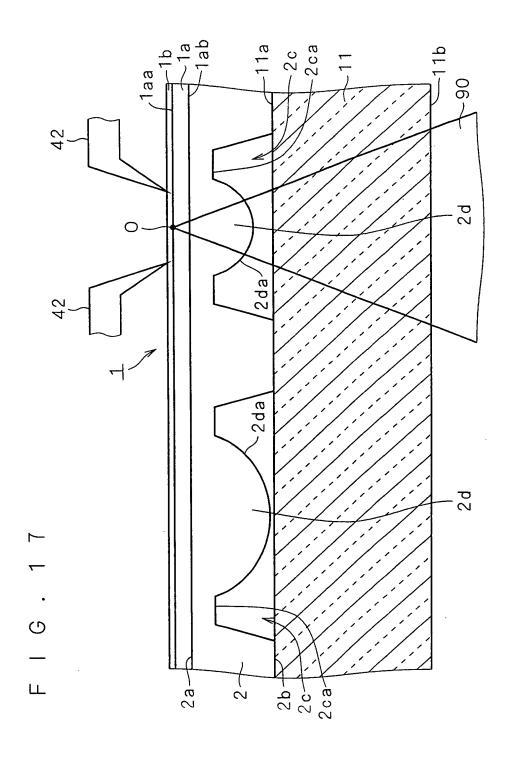
F I G . 1 4

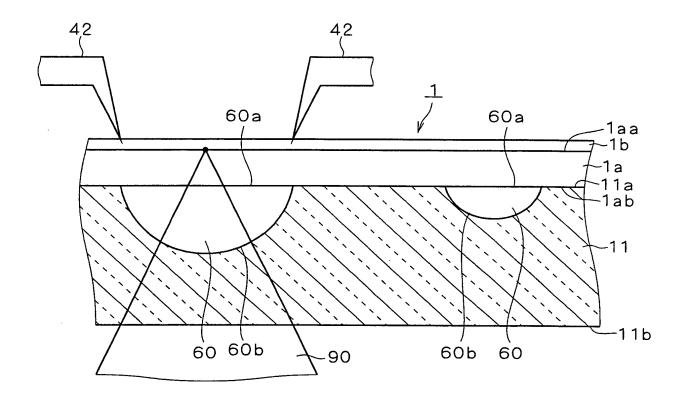


F I G . 15

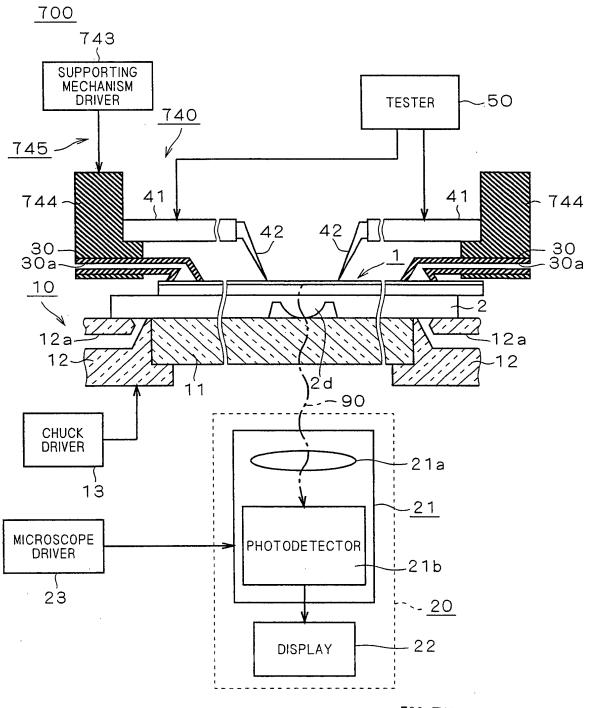








600: FAILURE ANALYZER 610: SIL DRIVER



700: FAILURE ANALYZER

740: PROBER

745: PROBE/SAMPLE DRIVER